CLAIMS

What is claimed is:

1. A digital decimation filter, including:

a programmable power supply for supplying power to electronic circuits of electronic equipment;

a integrator adapted to receive an input signal, the input signal including one or more frequency components;

a differentiator coupled to the integrator, the differentiator including a programmable counter;

a scaling unit coupled to the differentiator, the scaling unit adapted to produce an output signal; and

a control unit coupled to the integrator, the differentiator, and the scaling unit, the control unit adapted to store one or more programmable frequency notches, wherein the control unit activates the programmable counter such that the output signal is a filtered version of the input signal wherein the frequency components corresponding to the programmable frequency notches are attenuated.

2. The digital decimation filter of Claim 1, wherein the programmable counter is adapted to perform a function based on the input and a value stored in the differentiator, responsive to a signal from the control unit.

3. The digital decimation filter of Claim 2, wherein the function preformed by the programmable counter is a differentiation.

4. The digital decimation filter of Claim 1, wherein the control unit includes one or more registers, each register adapted to store a value, the value representing one of the programmable frequency notches.

5. The digital decimation filter of Claim 4, wherein the control unit further includes a data bus coupled to the registers, the data bus operable to load values from the registers or store values to the registers.

6. The digital decimation filter of Claim 4, wherein the control unit further includes:

a counter having a current value; and

one or more comparators, each comparator coupled to the counter and to one of the registers, each comparator operable to compare the value stored in one of the registers with the current value and produce an output, the output indicating whether the value stored in the register and the current value are equivalent.

7. The digital decimation filter of Claim 1, wherein the scaling unit includes:

a register, having an input adapted to receive data from the differentiator and an output;

a shifter coupled to the register, the shifter including a binary value, wherein the shifter is operable to shift the binary value; and

an adder coupled to the shifter, the adder adapted to produce an output.

8. A method of filtering a signal, including:

integrating the signal to produce an integrated signal;

selectively differentiating the integrated signal using a programmable counter to produce a differentiated signal, wherein the integrated signal is differentiated according to one or more programmable frequency notches; and

resampling the integrated signal at a frequency lower than a clock frequency.

9. The method of Claim 8, further including:

comparing a current value with one or more stored frequency notches; and

performing the differentiation if the current value is equal to a programmable frequency notches.

10. The method of Claim 8, further including scaling the differentiated signal to achieve a desired gain for a DC signal.

11. The method of Claim 10, wherein the desired gain is substantially 0 dB.

12. The method of Claim 10, wherein the scaling is accomplished using a register, a shifter, and an add/subtract unit.

13. The method of Claim 8, wherein the differentiation includes:

loading a first value from a first register;

selectively multiplying the first value by two;

selectively adding or subtracting the first value and a second value to produce a third value; and

storing the third value in a second register.

14. A delta-sigma analog-to-digital converter including:

a digital decimation filter, the digital decimation filter adapted to receive an input and produce an output;

wherein the digital decimation filter includes an integrator and a differentiator coupled together;

wherein the differentiator includes a programmable counter; and

wherein the programmable counter is adapted to selectively differentiate an input signal according to one or more programmable frequency notches.

15. The delta-sigma analog-to-digital converter of Claim 14, further including one or more registers adapted to store a programmable frequency notch.

16. The delta-sigma analog-to-digital converter of Claim 15, further including:

a counter having a current value;

a plurality of comparators, each comparator coupled to one of the registers and the counter, wherein each comparator is operable to compare the value of one of the registers with the current value and produce an output.

17. The delta-sigma analog-to-digital converter of Claim 14, further including:

a scaling unit coupled to the differentiator, the scaling unit operable to produce an output signal, wherein the output signal is a scaled version of the input.

18. The delta-sigma analog-to-digital converter of Claim 17, wherein the scaling unit has a gain of substantially 0 dB when a DC signal is input to the delta-sigma analog-to-digital converter.

19. The delta-sigma analog-to-digital converter of Claim 17, wherein the scaling unit includes a programmable shifter operable to shift data bitwise left or right.

20. A signal processing apparatus, including:

a integrator adapted to receive an input signal, the input signal including one or more frequency components;

a differentiator coupled to the integrator, the differentiator including a programmable counter;

a scaling unit coupled to the differentiator, the scaling unit adapted to produce an output signal; and

a control unit coupled to the integrator, the differentiator, and the scaling unit, the control unit adapted to store one or more programmable frequency notches, wherein the control unit activates the programmable counter such that the output signal is a filtered version of the input signal wherein the frequency components corresponding to the programmable frequency notches are attenuated.